Continuous-time delta-sigma modulator with inverting-amplifying chains

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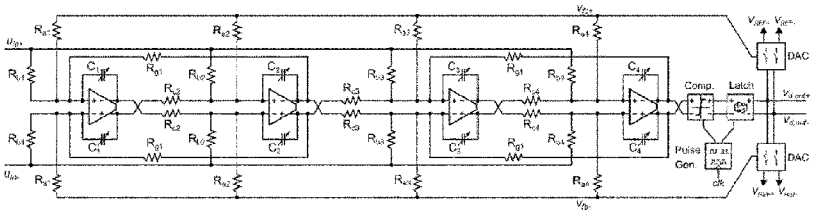

FIG. 1

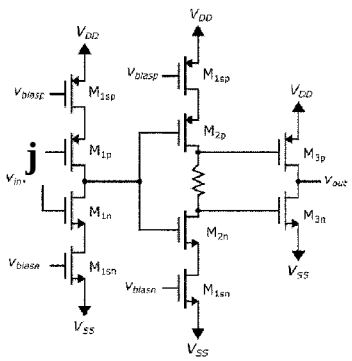

FIG. 5

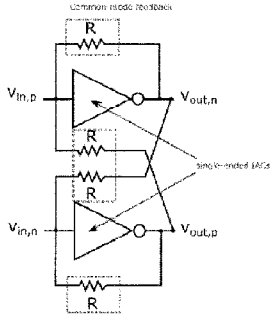

FIG. 6

(57) Abstract: The present disclosure relates to a continuous-time delta-sigma modulator for converting an analog input signal to a digital output signal, said continuous-time delta- sigma modulator comprising a gain stage in the form of at least one amplifying block comprising at least three serially connected inverting stages, wherein at least one of the inverting stages is an inverter, and wherein at least one inverting stage is configured to provide an amplification functionality, such that the serially connected inverting stages form a ring amplifier, said ring amplifier comprising an embedded voltage offset configured to stabilize the inverting stages, wherein the ring amplifier is configured to operate in continuous-time mode.

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Continuous-time delta-sigma modulator with inverting-amplifying chains

The present disclosure relates to the field of continuous-time delta-sigma analog-to-digital converters.

Background of invention

Delta-sigma analog-to-digital converters (ADC) are widely used in applications that demand high precision and accuracy. Delta-sigma ADCs oversample the desired signal, usually by a large factor, and filters the desired signal band. The basic principle of operation for a delta-sigma modulator involves a quantizer in a feedback loop for shaping the quantization noise such that most of the noise is shifted out of the band of interest. Discrete-time ADCs implemented using switched capacitor circuits have been used for decades in applications like biopotential, temperature measurements and digital processing of for example sound. More recently continuous-time delta-sigma ADCs have gained popularity in various high-speed, low-power applications.

Conventional continuous-time delta-sigma ADCs are implemented using operational-transconductance amplifiers (OTA). The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Because of their linear behavior, OTAs are well-suited for continuous-time applications. However, OTAs are also associated with a relatively high power consumption, and therefore typically dictate the power consumption of the continuous-time delta-sigma ADCs, and they do not scale well with technology advances in terms of for example transistor sizes.

Summary of invention

The present disclosure introduces an alternative approach to the conventional approach of using OTAs in continuous-time delta-sigma ADCs. By using several inverting stages, of which at least one is an inverter, for example in a ring-amplifier arrangement, a more power-efficient, area-efficient and more technology scalable solution than the OTA-based solution is obtained. In a first embodiment a continuous-time delta-sigma modulator for converting an analog input signal to a digital output signal is proposed, said continuous-time delta-sigma modulator comprising a gain stage in the form of an amplifying block comprising at least two serially connected inverting stages, wherein at least one inverting stage is an inverter, and wherein at

least one inverting stage is configured to provide an amplification, the inverting stages thereby forming an inverting-amplifying chain (IAC). 'Inverter' in this context may have the meaning of a variation of an inverter, such as a current-starved inverter. The OTAs of conventional continuous-time delta-sigma ADCs are not power and area efficient but do show a linear and controlled behavior and have therefore been the choice in continuous-time delta-sigma ADCs. The output of the integrators of continuous-time delta-sigma ADCs are sampled at a sample frequency f_s. Typical output voltages of integrators of a conventional OTA-based continuous-time delta-sigma ADC are shown in fig. 2. The sample frequency corresponds to a sampling at the end of every cycle. The present invention makes use of the fact that oscillation in the beginning and the middle of the sampling period may be acceptable as long as the output can be controlled such that it settles to an acceptable level within the sampling period.

Examples of this behavior are shown in figs. 11-13. Since continuous-time delta-sigma ADCs are sampled every period (after the loop filter), the oscillations do not affect its performance as long as the oscillations have settled within the sampling period. Consequently, as the inventors have realized, designs with more pronounced oscillations can still function, which allows the use of components and implementations, in particular a ring-amplifier, in a context (continuous-time) that they were originally not thought for. Several inverting-amplifiers, or combinations of inverting stages and inverters, can be cascaded to provide an amplifying functionality. Such implementations are conventionally used in discrete-time circuits due to their oscillation nature but are within the present disclosure proposed to operate in a continuous-time delta-sigma ADC. Despite the voltage shapes, wherein oscillations are allowed during the sampling cycle, the presently disclosed design may achieve the same quality as the previous designs with significant power savings. The continuous-time delta-sigma modulator according to the present disclosure may be arranged such that the amplifiers are not reset periodically.

One embodiment of the presently disclosed continuous-time delta-sigma modulator for converting an analog input signal to a digital output signal comprises three serially connected inverters, as shown in the ring amplifier in fig. 4B. A voltage output from the last inverter in the inverting-amplifying chain may be fed back, directly or indirectly, to a voltage input of the first inverter in the inverting-amplifying chain. Feedback may be applied to the inverting-amplifier chain. Examples of such feedback include resistor feedback, capacitor feedback and/or feedback using an amplifier stage. Ring amplifiers

are typically used in discrete-time in switched-capacitor circuits, successive approximation register and pipeline ADC since they are highly non-linear and complex. They are conventionally not used in continuous-time due to their oscillations. In discrete-time the amplifiers can be reset periodically. In the presently disclosed continuous-time delta-sigma modulator several inverting amplifiers may be cascaded and damped without being reset. Consequently, their properties can be turned into an advantage in delta-sigma ADC operating in continuous time since more power and area efficient circuits can be achieved.

The presently disclosed continuous-time delta-sigma ADC is configured to operate in continuous-time, which means that the sampling occurs after the loop filter part. This means that the loop filter (of fig. 8), in which the amplifying blocks, comprising at least two serially connected inverting stages, are located, operate on a continuous input signal and continuous output, without being reset. This is in contrast to discrete-time delta-sigma converters, for which the input signal is sampled prior to the loop filter. In a continuous-time delta-sigma ADC the input sampling may take place before the quantizer. The quantizer quantizes the sampled signal into a digital signal, which typically introduces quantization error noise. A feedback digital-to-analog converter (DAC) can be implemented in discrete time using a switched-capacitor circuit or in continuous-time using a current-steering DAC. The loop filter shapes the quantization noise out.

Description of drawings

Fig. 1 shows an example of an implementation of a continuous-time delta-sigma modulator. In the prior art solutions the amplification blocks are based on operational-transconductance amplifiers.

Fig. 2 shows the output voltages of prior art OTA-based integrators during operation of a continuous-time delta-sigma modulator.

Fig. 3 shows an example of a topology in an amplifying block used in the presently disclosed continuous-time delta-sigma ADC, the topology comprising two serially connected inverters.

Fig. 4 shows two further examples of topologies in an amplifying block used in the presently disclosed continuous-time delta-sigma ADC, the topologies comprising three serially connected inverters . Fig. 4A shows three cascaded inverters. Fig. 4B shows a ring amplifier. Both examples show a single-ended inverting-amplifying chain.

Fig. 5 shows a further example of a topology in an amplifying block used in the presently disclosed continuous-time delta-sigma ADC. The topology has three inverting stages with current limiters in the first and second stage and a dampening resistor.

Fig. 6 shows an example of a common mode feedback arrangement added around two amplifiers, arranged to adjust the DC level at the outputs, the setup thereby forming a pseudo-differential inverting-amplifier chain. The arrangement has two single-ended inverting amplifiers with common mode feedback implemented as 4 resistors.

Fig. 7 shows an example of a possible application of the presently disclosed continuous-time delta-sigma modulator in a receiving channel. In the example a low-noise amplifying block (LNA) is followed by an adaptive time gain control (A-TGC), the presently disclosed continuous-time delta-sigma ADC and a digital delay line (DD).

Fig. 8 shows an example of a system view of the presently disclosed continuous-time delta-sigma analog-to-digital converter, comprising a loop filter, a quantizer and a digital-to-analog converter (DAC). In a continuous-time delta-sigma converter, the loop filter operates on a continuous input signal and is sampled after the loop filter.

Fig. 9 shows an example of an implementation of a continuous-time delta-sigma ADC. The integrators are based on an inverting-amplifying chain.

Fig. 10 shows two parallel ring-amplifiers arranged as a pseudo-differential continuous-time ring-amplifier for use in for example the integrators of fig. 9

Fig. 11 shows an example of the output voltage of an integrator based on the amplifying block used in the presently disclosed continuous-time delta-sigma ADC.

Fig. 12 shows a further example of the output voltage of an integrator based on the amplifying block used in the presently disclosed continuous-time delta-sigma ADC.

Fig. 13 shows a further example of the output voltage of an integrator based on the amplifying block used in the presently disclosed continuous-time delta-sigma ADC.

Figs. 14a-c show OTA based integrator (fig. 14a), CT-RA based integrator (fig. 14b) and CT-RA example (fig. 14c).

Fig. 15 shows a schematic of exemplary continuous-time pseudo-differential ring amplifier topology, CTP-RA1 , which utilizes a capacitive stabilization load (C_{SL}) to achieve both small-signal and continuous-time transient stability.

Fig. 16 shows a schematic of another exemplary continuous-time pseudo-differential ring amplifier topology, CTP-RA2, which utilizes current starving to achieve both small-signal and continuous-time transient stability.

Figs. 17A-C show measured output spectra for a 3 MHz -6 dBFS differential input of ADC-RA1 (A), ADC-RA2 (B) and ADC-OTA (C). The fast Fourier transform is done with no-averaging, a Hanning window and 2^16 samples.

Fig. 18 shows a die micrograph of the measured chip. Only the pad openings of test structures and a dummy ADC-RA2 for the micrograph are not covered by metal-filling.
Fig. 19 shows examples of inverters: (a) traditional inverter, (b) double current starved inverter, (c) single current starved inverter, (d) inverter with split output. An inverter can be implemented in different ways and can be used a digital block or as an analog block.

Detailed description of the invention

The present disclosure relates to continuous-time delta-sigma modulator for converting an analog input signal to a digital output signal. The continuous-time delta-sigma modulator preferably comprises at least one gain stage in the form of at least one amplifying block comprising at least two serially connected inverting stages. At least one of the inverting stages may be configured to provide an amplification functionality. The inverting stages may thereby form an inverting-amplifying chain. The inverting-amplifying chains, which may also be referred to as inverting-amplifying chain amplifiers, used in the amplifying blocks according to the presently disclosed continuous-time delta-sigma modulator are simple amplifier implementations, which, however, are highly non-linear and generate complex transient response. This behavior may explain why operational-transconductance amplifiers are conventionally used in continuous-time delta-sigma modulators and inverting-amplifying chains are conventionally used in discrete-time systems.

In one embodiment of the presently disclosed continuous-time delta-sigma modulator for converting an analog input signal to a digital output signal, said continuous-time delta-sigma modulator comprises a gain stage in the form of at least one amplifying block comprising at least three serially connected inverting stages, wherein at least one of the inverting stages is an inverter, and wherein at least one inverting stage is configured to provide an amplification functionality, such that the serially connected inverting stages form a ring amplifier, said ring amplifier further comprising an embedded voltage offset configured to stabilize the inverting stages, and wherein the ring amplifier is configured to operate in continuous-time mode.

Preferably, the serially connected inverting stages are cascaded and configured provide an amplifying functionality. By having cascaded inverting stages, providing an amplifying functionality, an implementation is obtained which achieves a high gain and is difficult to control for a certain time, but if the signal is dampened during the sampling

cycle it may be controlled enough to settle to an acceptable level when the output signal is sampled.

A ring oscillator is a device composed of an odd number of inverters in a ring, whose output oscillates between two voltage levels. A ring amplifier is a small modular amplifier derived from a ring oscillator, which consists of cascaded inverting stages. A ring amplifier may be implemented in the form of a ring oscillator split into two signal paths embedding a different offset in each path. An example of a ring amplifier is shown in fig. 4B. An embedded offset (or deadzone) in the ring amplifier may stabilize the amplifier. The offset may be implemented as for example electrical resistance elements, switches or additional inverters. In order to use the ring amplifier with a feedback configuration, the feedback may be configured such that any input overshoot in the ring amplifier attenuates over each oscillation. The ring amplifier may thereby set a restriction on the feedback so that the ring amplifier and feedback are stable during continuous-time use. The inventors have found that this effect is particularly useful in the context of a continuous-time delta-sigma modulator for converting an analog input signal to a digital output signal. At least two or at least three serially connected amplifying inverters may form a ring amplifier configured to operate in continuous-time. A ring-amplifier in the presently disclosed context may be considered functionally equivalent to a continuous-time pseudo-differential OTA. The ring amplifier may comprise one or several voltage offsets embedded in the chain. In one embodiment a voltage output from the continuous-time delta-sigma modulator is fed back to a voltage input of the continuous-time delta-sigma modulator. The continuous-time delta-sigma modulator may comprise a digital-to-analog converter, wherein said digital-to-analog converter feeds back the voltage output of the continuous-time delta-sigma modulator to the voltage input of the loop filter comprising the inverting-amplifying chain. In a further embodiment of the continuous-time delta-sigma modulator, a voltage output from the last inverter in the inverting-amplifying chain is fed back to a voltage input of the first inverter in the inverting-amplifying chain. By having several inverting-amplifiers cascaded and fed back an efficient amplification is achieved which is dampened sufficiently before the continuous signal is sampled after the loop filter part of the modulator.

The present disclosure further relates to a method for amplifying a signal using continuous-time delta-sigma modulator having a gain stage in the form of at least one amplifying block comprising at least two serially connected inverting-amplifying stages.

The continuous-time delta-sigma ADC and the amplifying may be any of the proposed embodiment. In the method the signal is continuous in the loop filter and sampled at a sample frequency f_s after the loop filter. According to the method the amplifying block comprising at least two serially connected inverting-amplifying stages, preferably wherein the output of the last stage is fed back to the input of the first stage, is arranged to allow some initial oscillation compared to an ideal operational-transconductance amplifiers during the sampling cycle. The method involves continuous operation on a continuous analog input signal. Accordingly, the continuous-time delta-sigma modulator may be arranged to operate continuously on a continuous analog input signal. During the cycle the arrangement and the dampening nature of a ring-amplifier, the signal settles to a level which is close a corresponding behavior of an operational-transconductance amplifier. Examples of such behavior for the presently disclosed inverting-amplifier chain are shown in figs 11-13. The behavior of a corresponding OTA-based prior art implementation is shown in fig. 2. As can be seen, these integrators are very linear and have very controlled behavior and a well-defined triangular shape during operation. Depending on how strict the oscillation vs. dampening requirements are set the presently disclosed implementation may be made less power consuming. Typically, if more oscillation and less stability is acceptable for achieving a good deviation level when the signal is sampled, the power consumption will be lower. Despite the voltage shapes, the presently disclosed design may achieve the same quality as the previous designs with significant power savings.

In one embodiment the continuous-time delta-sigma ADC comprises at least three serially connected inverting stages. Preferably, at least two of the inverting stages are inverters, which may be implemented using two complementary transistors in a CMOS configuration. In one embodiment, at least three of the inverting stages are inverters.

Single-ended in the context of ADC refers to using one input for the signal. In pseudo differential mode a second input and a second output are used in a configuration as shown in fig. 6. The
voltage applied to the second input provides an offset from ground or a pseudo ground for the first input. In the presently disclosed continuous-time delta-sigma modulator the amplifying block may comprise two single-ended lACs and a common mode feedback (CMFB), providing a differential or a pseudo differential system. Fig. 6 shows an example of such an implementation, implemented with 4 resistors.

Preferably at least one, at least two, at least three, or each inverting stage is configured to provide an amplification functionality.

The inverting stages may be implemented as CMOS inverting stages, such as CMOS inverters, preferably with amplifying functionality. Alternatively, or in combination, the serially connected inverting stages comprise a pair of P-channel and N-channel MOS output transistors connected in series between a power source voltage node and a ground node. The topology may comprise an electrical resistance element between outputs of at least one of the pairs of output transistors, such as in a second inverting stage of the three serially connected inverting stages. The resistance element may be arranged to control dampening and/or oscillation of the gain stage comprising the serially connected inverting stages, such as three serially connected inverting stages.

In the embodiment comprising a pair of P-channel and N-channel MOS output transistors connected in series between a power source voltage node and a ground node, the output of one P-channel of one inverting stage, such as the second inverting stage, may be connected to the input of a P-channel of a following inverting stage in the inverting-amplifying chain. Similarly the output of one N-channel of the inverter may be connected to the input of the N-channel of the following inverter.

The inverting-amplifying stages may further comprise current limiters as shown in the first and second stage of the topology of fig. 5.

As explained above, the difference between discrete-time delta-sigma converters and continuous-time delta-sigma converters is that in discrete-time the signal is sampled before the filter and in continuous-time the signal is sampled after the filter. Hence, a continuous-time delta-sigma ADC involves sampling of the output signal of the gain stage. Therefore, the sampling period can be used to dampen the oscillating signal. In one embodiment an oscillating output of the last of the inverting stages is sampled at a sample frequency having a sampling period, wherein the at least two serially connected inverting stages are arranged to dampen the oscillations of the output below a predefined tolerance level within the sampling period. Even an implementation in which the output signal does not settle completely within the sampling period may achieve the same quality as the OTA-based prior art implementations with significant power savings.

Ring amplifiers are typically used in discrete-time systems such as switched capacitor circuits. Typically they are reset on one phase and operate functionally on the other phase. The continuous-time delta-sigma modulator according to the present disclosure may be arranged such that the gain stage comprising the at least three serially connected inverting stages operates continuously without resetting said gain stage.

Preferably, the presently disclosed continuous-time delta-sigma modulator is configured to minimize non-linear behavior of the serially connected inverting stages. This may be achieved for example by the above-mentioned dampening resistor(s) and/or the last inverter in the inverting-amplifying chain being fed back to a voltage input of the first inverter in the inverting-amplifying chain. The may be the case of for example a ring-amplifier. The minimization of non-linear and/or transient behavior of the serially connected inverting stages may be done in relation to use in a specific application and technology, and/or for a specific gain.

The presently disclosed continuous-time delta-sigma ADC may be of any order, i.e. any number of integrators and feedback loops, such as a first order, second order, third order, fourth order modulator, may be used.

One embodiment of the continuous-time delta-sigma ADC comprises a gain stage in the form of an amplifying block comprising at least three serially connected inverting stages is arranged to produce an amplified output signal having initial oscillation below a predefined tolerance level with respect to a reference gain, subsequently dampened to a minimum tolerance level of oscillation with respect to the reference gain.

The presently disclosed ADC may be used in a range of applications. For example the continuous-time delta-sigma modulator may be used in an electronic device comprising means for converting an analog signal, such as a signal comprising sound or light, into a digital signal, such as in a hearing aid or a mobile phone. The ADC may also be used in music or any other sound processing applications. In principle ADC are used for any application where analog signals are sampled and processed in digital form. The continuous-time delta-sigma ADC may be used in low signal-to-noise ratios, for example for an input signal having a low signal-to-noise ratio, preferably less than 60 dB, more preferably less than 50 dB, even more preferably less than 40 dB. The continuous-time delta-sigma ADC may be used in higher signal-to-noise ratios, for example in hearing aids and/or mobile phones.

Detailed description of drawings

The invention will in the following be described in greater detail with reference to the accompanying drawings. The drawings are exemplary and are intended to illustrate some of the features of the presently disclosed continuous-time delta-sigma analog-to-digital converters, and are not to be construed as limiting to the presently disclosed invention.

Fig. 1 shows an example of an implementation of a continuous-time delta-sigma modulator. In the prior art solutions the integrators are based on operational-transconductance amplifiers. The disclosed continuous-time delta-sigma modulator is a fourth order loop filter.

Fig. 2 shows an example of output voltages of prior art OTA-based integrators during operation of a continuous-time delta-sigma modulator. The output voltages of the OTA-based integrators during operation of the CTDSM have a triangular shape, as shown in the figure. The integrators are very linear and have very controlled behaviour. The output voltages are sampled at the end of each sample cycle i.e. at the top and bottom peaks.

Fig. 3 shows an example of a topology in an amplifying block used in the presently disclosed continuous-time delta-sigma ADC, the topology comprising two serially connected inverters implemented as two serially connected pairs of transistors. A dampening resistance element is arranged between M_{2p} and M_{2n}.

Fig. 4 shows two further examples of topologies in an amplifying block used in the presently disclosed continuous-time delta-sigma ADC, the topologies comprising three serially connected inverters . Fig. 4A shows three cascaded inverters. Fig. 4B shows a ring amplifier. Both examples show a single-ended inverting-amplifying chain.

Fig. 5 shows a further example of a topology in an amplifying block used in the presently disclosed continuous-time delta-sigma ADC. The topology has three inverting stages with current limiters (M_{1sp}, M_{1sn}) in the first and second stage and a dampening resistor in the second stage.

Fig. 6 shows an example of a common mode feedback arrangement added around two amplifiers, arranged to adjust the DC level at the outputs. The arrangement has two single-ended inverting amplifiers with common mode feedback implemented as 4 resistors (R).

Fig. 7 shows an example of a possible application of the presently disclosed continuous-time delta-sigma modulator in a receiving channel of an ultrasound system. In the example a low-noise amplifying block (LNA) is followed by an adaptive time gain control (A-TGC), the presently disclosed continuous-time delta-sigma ADC and a digital delay line (DD). Similar setups may be used in other applications.

Fig. 8 shows an example of a system view of the presently disclosed continuous-time delta-sigma analog-to-digital converter, comprising a loop filter, a quantizer and a digital-to-analog converter (DAC). In a continuous-time delta-sigma converter, the loop filter operates on a continuous input signal and is sampled after the loop filter. The conversion involves quantization of the input, which introduces a small amount of error.

Fig. 9 shows an example of an implementation of a continuous-time delta-sigma ADC. The continuous-time delta-sigma modulator is a fourth order loop filter. The integrators are based on pseudo-differential inverting-amplifying chains.

Fig. 10 shows two parallel ring-amplifiers arranged as a pseudo-differential continuous-time ring-amplifier for use in for example the integrators of fig. 9

Fig. 11 shows an example of the output voltage of an integrator based on the amplifying block used in the presently disclosed continuous-time delta-sigma ADC. This integrator based on the new amplifying block comprising at least two serially connected inverting stages has a less linear behaviour, but is nevertheless controllable. It tracks the traditional triangular shape from fig. 2 but with dampened oscillations. In the highlighted area it can be seen that the oscillations are highest in the beginning of the cycle. Since CTDSM are sampled every period, corresponding to the distinguished high and low peaks, the oscillations during the cycle do not affect its performance as long as the oscillations have settled within the sampling period. Consequently, designs with more pronounced oscillations can still function.

Fig. 12 shows a further example of the output voltage of an integrator based on the amplifying block used in the presently disclosed continuous-time delta-sigma ADC. This implementation has an even more pronounced oscillation but also a lower power-consumption since less power is used for tracking the ideal triangular shape. Despite the voltage shapes, this design achieves the same quality as the previous designs with further improved power savings.

Fig. 13 shows a further example of the output voltage of an integrator based on the amplifying block used in the presently disclosed continuous-time delta-sigma ADC. The design of this example has been further pushed in terms of allowed oscillations. In this case, the output voltage does not fully settle within a clock period Ts, however, the error generated is small enough to not compromise the performance of the continuous-time delta-sigma ADC.

Figs. 14a-c show an example of an active RC-integrator based on CT-RA as an alternative to traditional OTAs. The OTA based integrator is shown in fig. 14a, CT-RA based integrator is shown in fig. 14b and a CT-RA example is shown in fig. 14c.

Examples

Two continuous-time pseudo-differential ring amplifiers (CTP-RA), CTP-RA1 and CTP-RA2 are exemplified herein. The designs operate in continuous time (CT), do not need to be periodically reset and maintain the inherent advantages of ring amplifiers (RA). A prototype has been fabricated in a 65nm CMOS process which contains two versions of a continuous-time delta-sigma ADC using the two designs presented. The best design proposed consumes 135 µW and achieves a FoMW of 33.7 fJ/conv.-step, outperforming the SotA delta-sigma ADCs for that specification rage. Moreover, it consumes 70% less power and achives a 78% better FoMw than its OTA-based ADC counterpart, ADC-OTA

The structure of CTP-RA1 is shown in Fig. 15. It consists of two single-ended CT RAs, a CT common-mode feedback (CMFB) and a capacitive stabilization load (CSL). The single-ended RAs contain three gain stages, and the stabilizing offset is embedded in the second stage using $R_{sp}i_t$. The last stage is constructed using high V, transistors for higher output resistance and to increase the robustness to process, voltage and temperature variations [2]. The last stage transistors are sized to supply any dc current

load required. A passive resistor-based CMFB is used for simplicity. The CSL is added to achieve stability in CT operation. Firstly, it creates a dominant pole that improves the phase margin (PM) of the CTP-RA. Secondly, it limits the output slew rate (SR) to ensure that input overshoots decrease in each successive oscillation [2].

The structure of the CTP-RA2 is shown in Fig. 16. It consists of two single-ended RAs and the same passive CMFB as CTP-RA1 . The single-ended RAs have the same gain structure as CTP-RA1 . However, they achieve stability by current starving the first two stages instead of using a stabilization load. Reducing the current of the first two stages decreases the transconductance of the transistors, which improves the PM. Furthermore, it also decreases the gain and limits the SR of the first two stages, achieving transient stability.

As a proof of concept, both designs, CTP-RA1 and CTP-RA2, are used to implement two versions of a continuous-time delta-sigma (CTDS) analog-to-digital converter (ADC) in a 65nm process, ADC-RA1 and ADC-RA2. The ADC is also implemented using symmetrical OTAs, ADC-OTA, to accurately compare the performance of the proposed RAs. The ADCs are specified for beamforming ultrasound applications with an 8 MHz bandwidth (BW), a 320 MHz sampling frequency (fs), 1-bit output and a required 48 dB signal-to-noise and distortion ratio (SNDR). The ADC, shown in Fig. 1, has a 4^{th} order cascade-of-resonators feedback structure. The loop filter consists of four active RC integrators and resistive filter coefficients. The single-bit quantizer consists of a clocked comparator, a clocked latch and a pulse generator that creates the clock signals. Two one-bit digital-to-analog converters (DACs) provide the voltage feedback signals for the loop filter. The three ADC implementations have identical quantizer and DACs. However, the four integrators have been implemented using CTP-RA1 , CTP-RA2 and a traditional symmetrical OTA respectively.

The prototype die containing ADC-RA1 , ADC-RA2 and ADC-OTA, is fabricated in a 65nm CMOS process. Due to the scalability of the presented CTP-RAs, ADC-RA1 and ADC-RA2 can operate at a supply of 1.1 V, which is lower than the typical 1.2 V supply of the process used. The designs consume 261 μW, 153 μW and 511 μW, and achieve 52.0 dB, 50.8 dB and 48.1 dB SNDR for an 8 MHz BW, respectively. The measured spectra for a 3 MHz, -6 dBFS differential input can be seen in Fig. 17.

The performance of ADC-RA1 and ADC-RA2 is compared to ADC-OTA, and to state-of-the-art (SotA) delta-sigma ADCs in the same range of specifications in table 1 below.

	ADC-RA1	ADC-RA2	ADC-OTA	[3]	***[4]	[5]	[6]
Technology	65 nm CMOS			65 nm	65 nm	40 nm	55 nm
Year	2018			2016	2018	2012	2015
ADC architecture	CTDS-RA	CTDS-RA	CTDS-OTA	DTDS-RA	CTDS-RA	CTDS-OTA	CTDS-OTA
V_{DD} [V]	1.1	1.1	1.2	1.2	0.9	-	1.2 / 1.8
BW [MHz]	8	8	8	1	1	10	2.2
f_s [MHz]	320	320	320	102.4	104	300	140
SNDR [dB]	52.0	50.8	48.1	62.0	61.7	70	90.4
Power [µW]	261	153	511	1000	490	2570	4500
Area [mm^2]	0.0162	0.0151	0.0170	0.0252	-	0.0510	0.0900
*FoM_W [fJ/conv.-step]	50.1	33.7	153.9	483	247	50.0	37.8

Table 1

$*\ FoM_W = Power/\ (2 \cdot BW \cdot 2^{(SNDR - 1.76)/6.02})$

** *Traditional OTA-based ADC implementation added for comparison accuracy.*

*** *Simulation results*

The best design proposed consumes 153 µW and achieves a FoM_W of 33.7 fJ/conv.-step, which outperforms the SotA delta-sigma ADCs for that specification range and is 78% superior to its traditional OTA-based ADC counterpart.

References

[1] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U. Moon, "Ring Amplifiers for Switched Capacitor Circuits," *IEEE JSSC,* vol. 47, no. 12, pp. 2928-2942, Dec. 2012.

[2] Y. Lim and M. P. Flynn, "A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifier," *IEEE JSSC,* vol. 50, no. 10, pp. 2331-2341 , Oct. 2015.

[3] T. Suguro and I. Hiroki, "Low power DT delta-sigma modulator with ring amplifier SC-integrator," *ISCAS,* pp. 2006-2009, May 2016.

[4] A. S. Ahmed, M. M. Aboudina and F. A. Hussein, "A Ring Amplifier Architecture for Continuous-Time Applications," *ISCAS,* pp. 1-5, May 2018.

[5] K. Matsukawa and K. Obata, "A 10 MHz BW 50 fJ/conv. continuous time ΔΣ modulator with high-order single opamp integrator using optimization-based design method," *VLSIC,* pp. 160-161, July 2012.

[6] C. Ho, C. Liu, C. Lo, H. Tsai, T. Wang and Y. Lin, "A 4.5 mW CT Self-Coupled ΔΣ Modulator With 2.2 MHz BW and 90.4 dB SNDR Using Residual ELD Compensation," *IEEE JSSC,* vol. 50, no. 12, pp. 2870-2879, Dec. 2015.

Further details of the invention

1. A continuous-time delta-sigma modulator for converting an analog input signal to a digital output signal, said continuous-time delta-sigma modulator comprising a gain stage in the form of at least one amplifying block comprising at least two serially connected inverting stages, wherein at least one of the inverting stage is an inverter, and wherein at least one inverting stage is configured to provide an amplification functionality, the inverting stages thereby forming an inverting-amplifying chain.

2. The continuous-time delta-sigma modulator according to any of the preceding items, comprising at least three serially connected inverting stages.

3. The continuous-time delta-sigma modulator according to any of the preceding items, wherein at least two of the inverting stages are inverters.

4. The continuous-time delta-sigma modulator according to item 2, wherein at least three of the inverting stages are inverters.

5. The continuous-time delta-sigma modulator according to any of the preceding items, wherein a voltage output from the last inverter in the inverting-amplifying chain is fed back, directly or indirectly, to a voltage input of the first inverter in the inverting-amplifying chain.

6. The continuous-time delta-sigma modulator according to any of the preceding items, wherein each inverting stage is configured to provide an amplification functionality.

7. The continuous-time delta-sigma modulator according to any of the preceding items, wherein at least two or at least three serially connected inverters form a ring amplifier configured to operate in continuous-time.

8. The continuous-time delta-sigma modulator according to item 7, wherein the ring amplifier comprises a voltage offset embedded in the chain.

9. The continuous-time delta-sigma modulator according to any of the preceding items, wherein the inverting stages are CMOS inverting stages, such as CMOS inverters, preferably as pairs of complementary CMOS transistors in a CMOS configuration.

10. The continuous-time delta-sigma modulator according to any of the preceding items, wherein each serially connected inverting stage comprises a pair of P-channel and N-channel MOS output transistors connected in series between a power source voltage node and a ground node.

11. The continuous-time delta-sigma modulator according to item 10, wherein an output of one P-channel of one inverting stage, such as the second inverting stage, is connected to the input of a P-channel of a following inverting stage in the inverting-amplifying chain, and wherein an output of one N-channel of the inverter is connected to the input of the N-channel of the following inverter.

12. The continuous-time delta-sigma modulator according to any of the preceding items, further comprising an electrical resistance element between outputs of at least one of the pairs of output transistors, such as in a second inverting stage of the three serially connected inverting stages.

13. The continuous-time delta-sigma modulator according to any of items 12, wherein the resistance element is arranged to control dampening and/or oscillation of the gain stage comprising the at least three serially connected inverting stages.

14. The continuous-time delta-sigma modulator according to any of the preceding items, wherein an oscillating output of the last of the inverting stages is sampled at a sample frequency having a corresponding sampling period, and wherein

the at least two serially connected inverting stages are arranged to dampen the oscillations of the output below a predefined tolerance level within the sampling period.

15. The continuous-time delta-sigma modulator according to any of the preceding items, said modulator arranged to operate continuously on a continuous analog input signal.

16. The continuous-time delta-sigma modulator according to any of the preceding items, said modulator arranged such that the gain stage comprising the at least three serially connected inverting stages operates continuously without resetting said gain stage.

17. The continuous-time delta-sigma modulator according to any of the preceding items, wherein said modulator is configured to minimize non-linear behavior of the serially connected inverting stages.

18. The continuous-time delta-sigma modulator according to any of the preceding items, wherein the serially connected inverting stages are arranged to minimize their non-linear and/or transient behavior for use in a specific application and technology, and/or for a specific gain.

19. The continuous-time delta-sigma modulator according to any of the preceding items, wherein the serially connected inverting stages are cascaded to provide an amplifying functionality.

20. The continuous-time delta-sigma modulator according to any of the preceding items, wherein the gain stage in the form of an amplifying block comprising at least three serially connected inverting stages is arranged to produce an amplified output signal having initial oscillation below a predefined tolerance level with respect to a reference gain, subsequently dampened to a minimum tolerance of oscillation with respect to the reference gain.

21. The continuous-time delta-sigma modulator according to any of items 19-20, wherein the serially connected cascaded inverting stages are configured to operate in continuous-time amplification mode.

22. Use of the continuous-time delta-sigma modulator according to any of the preceding items for an input signal having a low signal-to-noise ratio, preferably less than 60 dB, more preferably less than 50 dB, even more preferably less than 40 dB.

23. Use of the continuous-time delta-sigma modulator according to any of items 1-21 in an electronic device comprising means for converting an analog signal, such as a signal comprising sound or light, into a digital signal, such as a hearing aid or a mobile phone.

Claims

1. A continuous-time delta-sigma modulator for converting an analog input signal to a digital output signal, said continuous-time delta-sigma modulator comprising a gain stage in the form of at least one amplifying block comprising at least three serially connected inverting stages, wherein at least one of the inverting stages is an inverter, and wherein at least one inverting stage is configured to provide an amplification functionality, such that the serially connected inverting stages form a ring amplifier, said ring amplifier comprising an embedded voltage offset configured to stabilize the inverting stages, wherein the ring amplifier is configured to operate in continuous-time mode.

2. The continuous-time delta-sigma modulator according to claim 1, wherein a voltage output from the continuous-time delta-sigma modulator is fed back to a voltage input of the continuous-time delta-sigma modulator.

3. The continuous-time delta-sigma modulator according to claim 2, further comprising a digital-to-analog converter, wherein said digital-to-analog converter feeds back the voltage output to the voltage input.

4. The continuous-time delta-sigma modulator according to any of claims 1-3, wherein at least two of the inverting stages are inverters.

5. The continuous-time delta-sigma modulator according to any of the preceding claims, wherein each inverting stage is configured to provide an amplification functionality.

6. The continuous-time delta-sigma modulator according to any of the preceding claims, wherein the embedded offset is an electrical resistance element between outputs of at least one of the pairs of output transistors, such as in a second inverting stage of the three serially connected inverting stages.

7. The continuous-time delta-sigma modulator according to claim 6, wherein the resistance element is arranged to control dampening and/or oscillation of the gain stage comprising the at least three serially connected inverting stages.

8. The continuous-time delta-sigma modulator according to any of the preceding claims, wherein an oscillating output of the last of the inverting stages is sampled at a sample frequency having a corresponding sampling period,

9. The continuous-time delta-sigma modulator according to any of the preceding claims, wherein the at least three serially connected inverting stages are arranged to dampen the oscillations of the output below a predefined tolerance level within the sampling period.

10. The continuous-time delta-sigma modulator according to any of the preceding claims, said modulator arranged to operate continuously on a continuous analog input signal.

11. The continuous-time delta-sigma modulator according to any of the preceding claims, said modulator arranged such that the gain stage comprising the at least three serially connected inverting stages operates continuously without resetting said gain stage.

12. The continuous-time delta-sigma modulator according to any of the preceding claims, wherein said modulator is configured to minimize non-linear behavior of the serially connected inverting stages.

13. The continuous-time delta-sigma modulator according to any of the preceding claims, wherein the serially connected inverting stages are cascaded to provide an amplifying functionality.

14. The continuous-time delta-sigma modulator according to any of the preceding claims, wherein the gain stage in the form of an amplifying block comprising at least three serially connected inverting stages is arranged to produce an amplified output signal having initial oscillation below a predefined tolerance level with respect to a reference gain, subsequently dampened to a minimum tolerance of oscillation with respect to the reference gain.

15. Use of the continuous-time delta-sigma modulator according to any of claims 1-14 in an electronic device comprising means for converting an analog signal,

such as a signal comprising sound or light, into a digital signal, such as a hearing aid or a mobile phone.

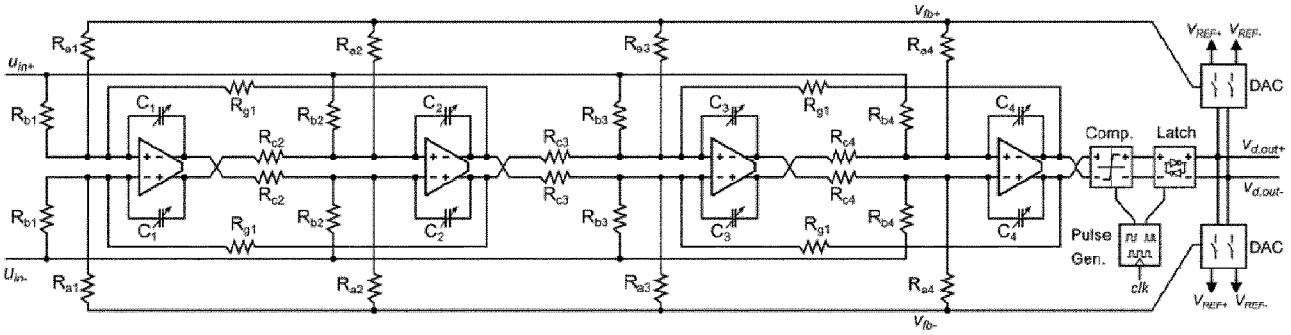


FIG. 1

PRIOR ART

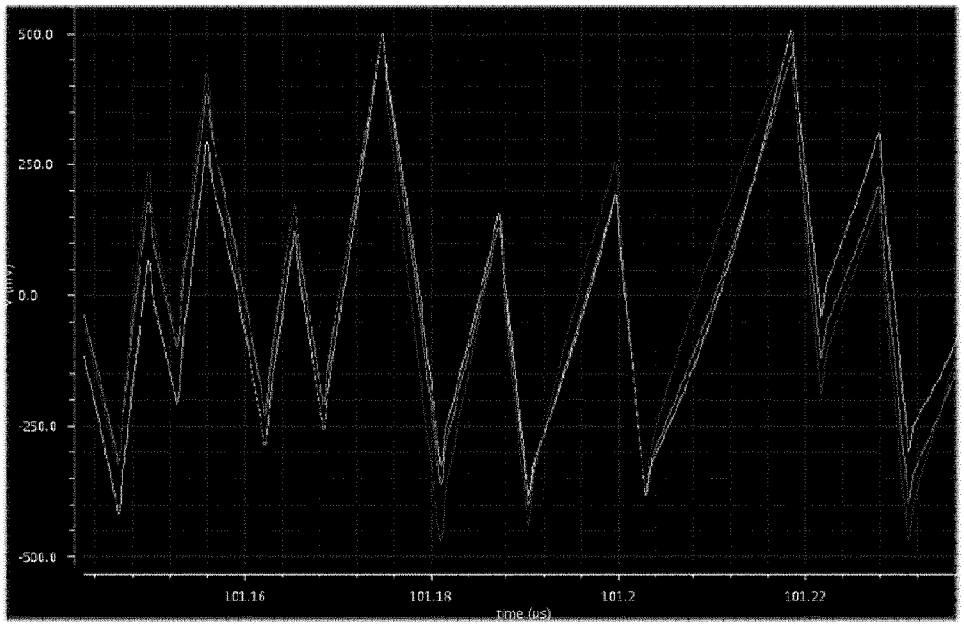


FIG. 2

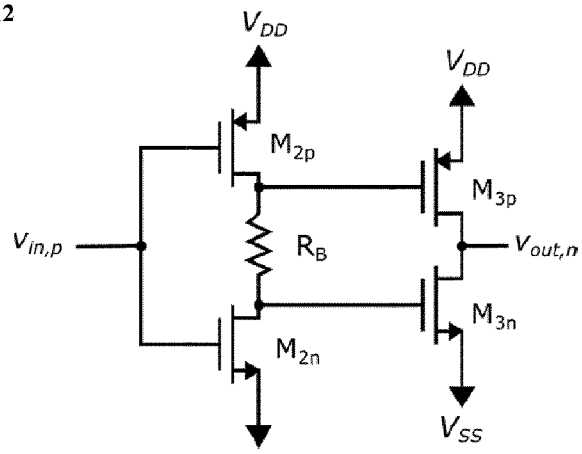
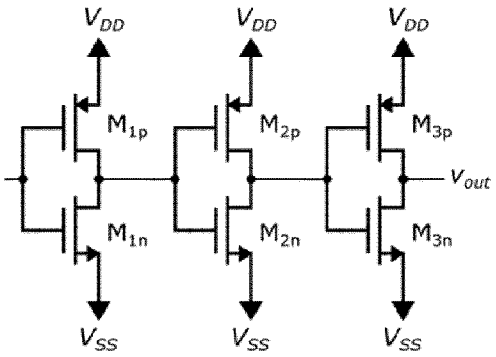

V_{DD}
V_{DD}
M_{2p}
M_{3p}
$V_{in,p}$
R_B
$V_{out,n}$
M_{3n}
M_{2n}
V_{SS}

FIG. 3


V_{DD}
V_{DD}
V_{DD}
M_{1p}
M_{2p}
M_{3p}
V_{out}
M_{1n}
M_{2n}
M_{3n}
V_{SS}
V_{SS}
V_{SS}

a)

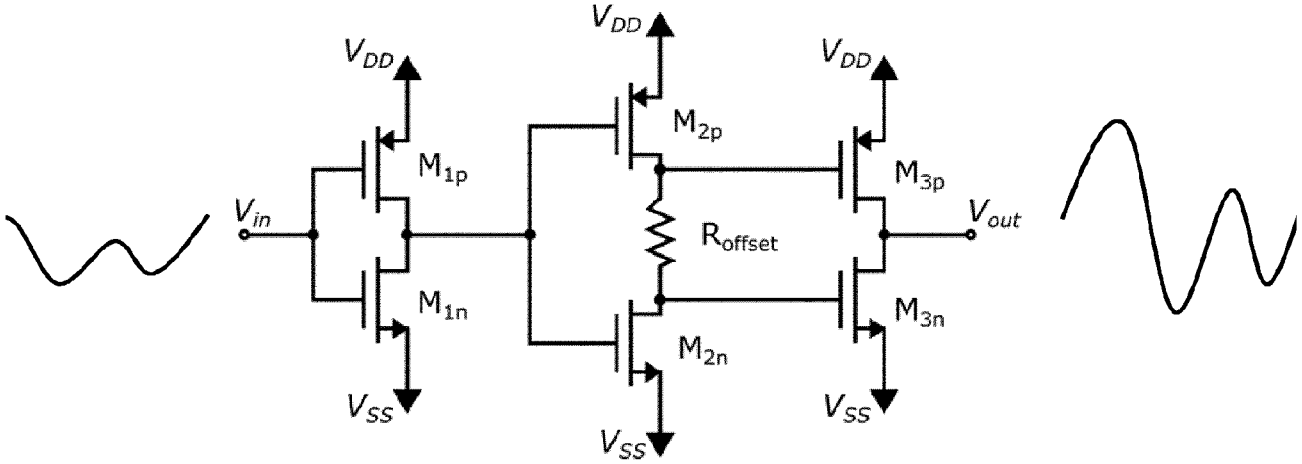

V_{DD}
V_{DD}
V_{DD}
M_{2p}
V_{DD}
M_{1p}
M_{3p}
V_{in}
R_{offset}
V_{out}
M_{1n}
M_{3n}
M_{2n}
V_{SS}
V_{SS}
V_{SS}

FIG. 4

b)

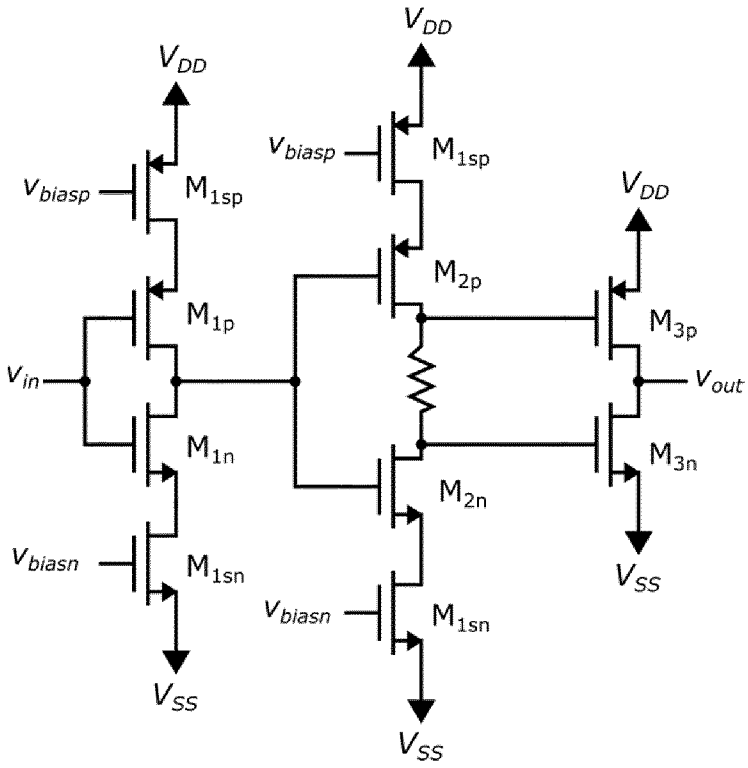

V_{DD}
V_{biasp}
M_{1sp}
M_{1p}
V_{in}
M_{1n}
V_{biasn}
M_{1sn}
V_{SS}
V_{DD}
V_{biasp}
M_{1sp}
M_{2p}
M_{2n}
V_{biasn}
M_{1sn}
V_{SS}
V_{DD}
M_{3p}
V_{out}
M_{3n}
V_{SS}

FIG. 5

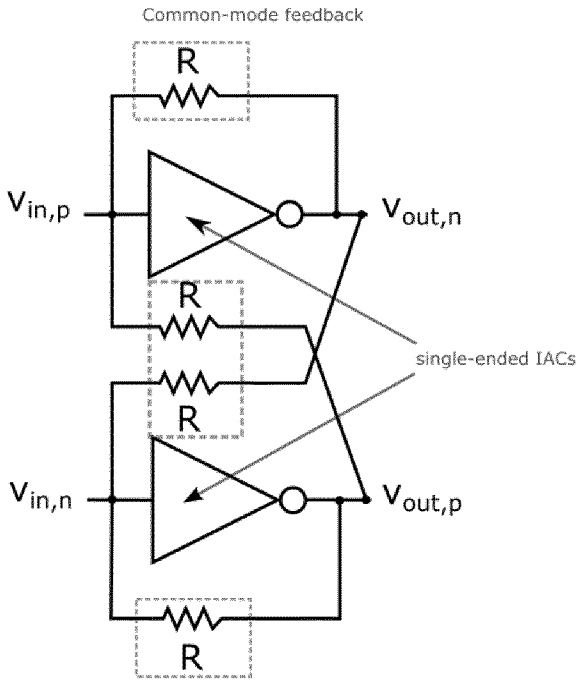

Common-mode feedback
R
$V_{in,p}$
$V_{out,n}$
R
R
single-ended IACs
$V_{in,n}$
$V_{out,p}$
R

FIG. 6

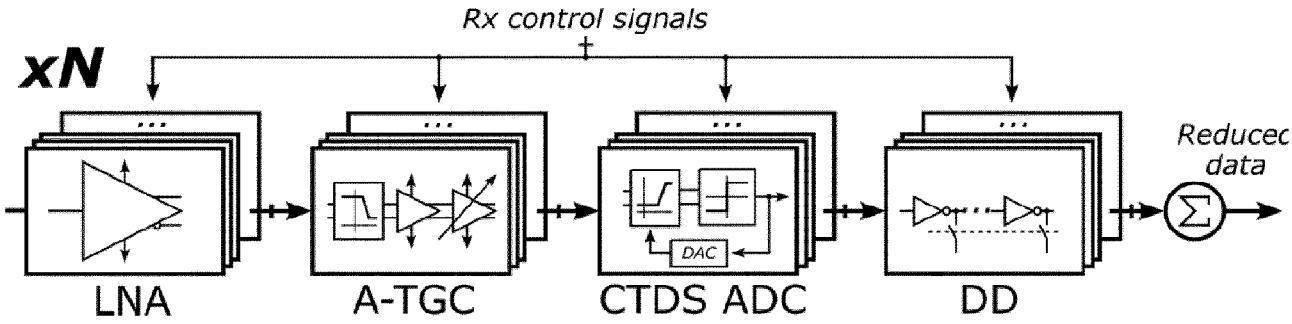

Rx control signals
xN
Reducec
data
DAC
LNA
A-TGC
CTDS ADC
DD

FIG. 7

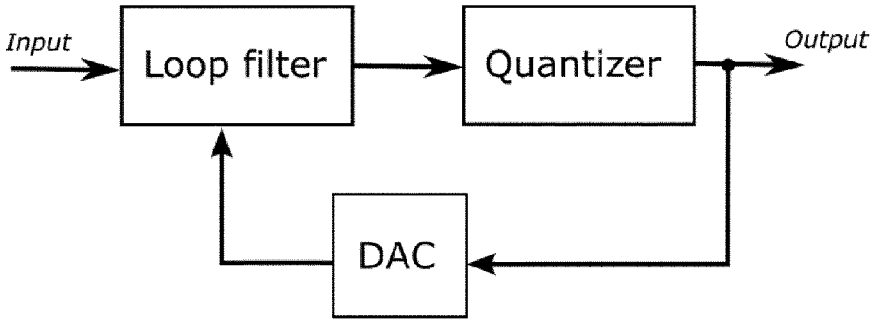

Input
Loop filter
Quantizer
Output
DAC

FIG. 8

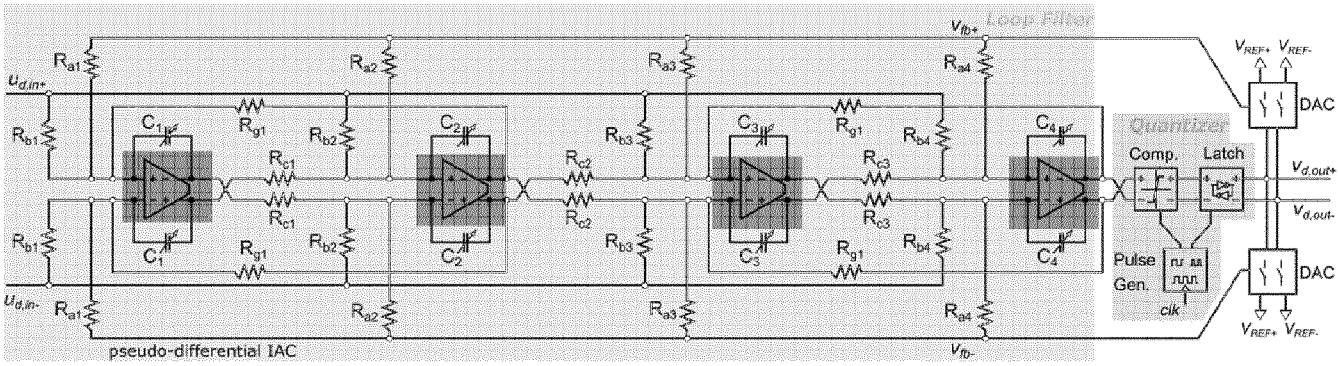


FIG. 9

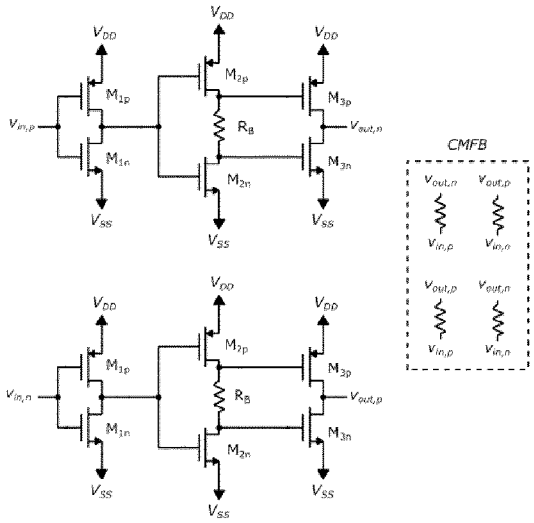


FIG. 10

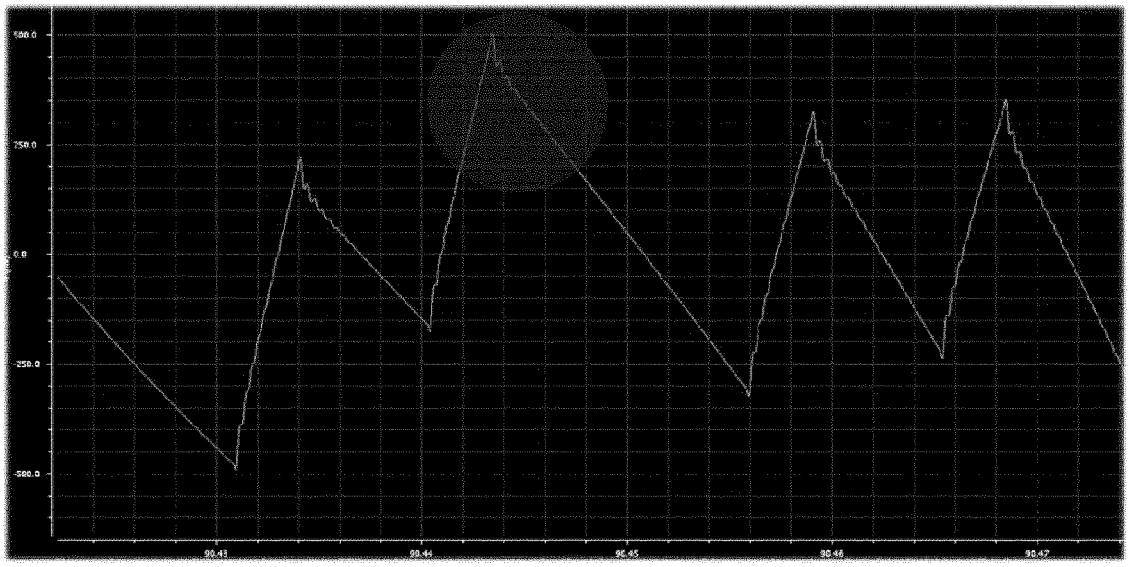


FIG. 11

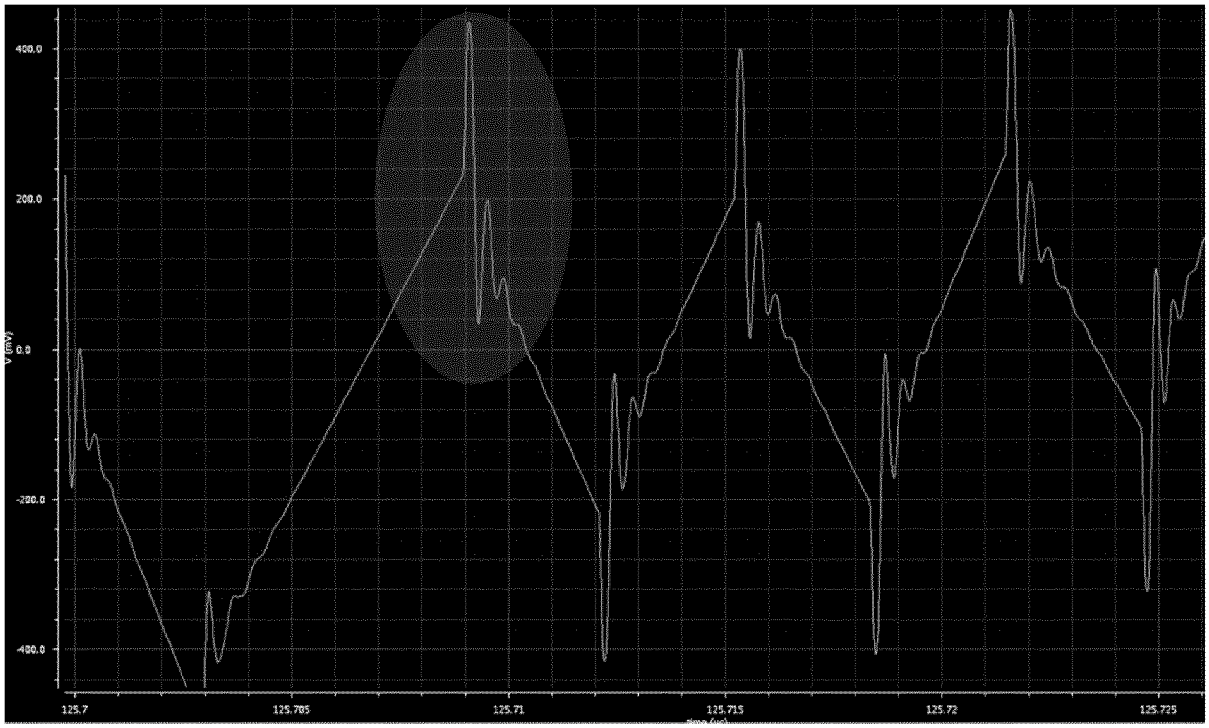

400.0
200.0
0.0
-200.0
-400.0
V (mV)
125.7
125.705
125.71
125.715
125.72
125.725

FIG. 12

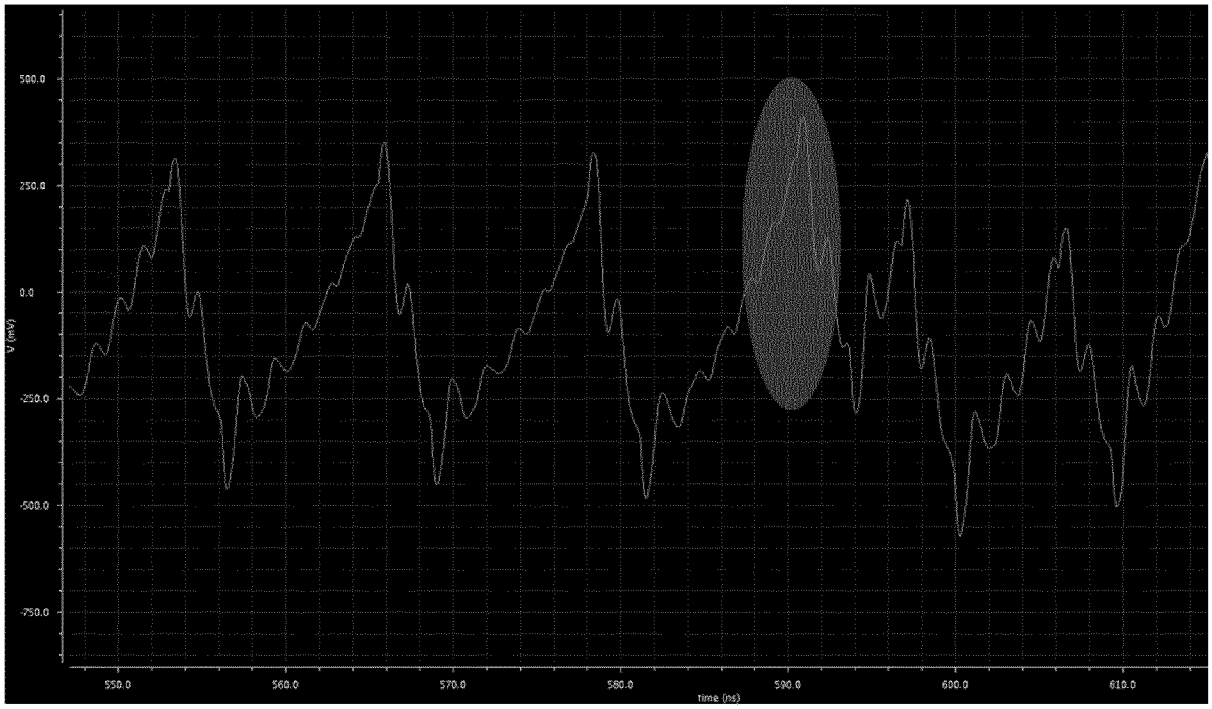

500.0
250.0
0.0
-250.0
-500.0
-750.0
V (mV)
550.0
560.0
570.0
580.0
590.0
600.0
610.0
time (ns)

FIG. 13

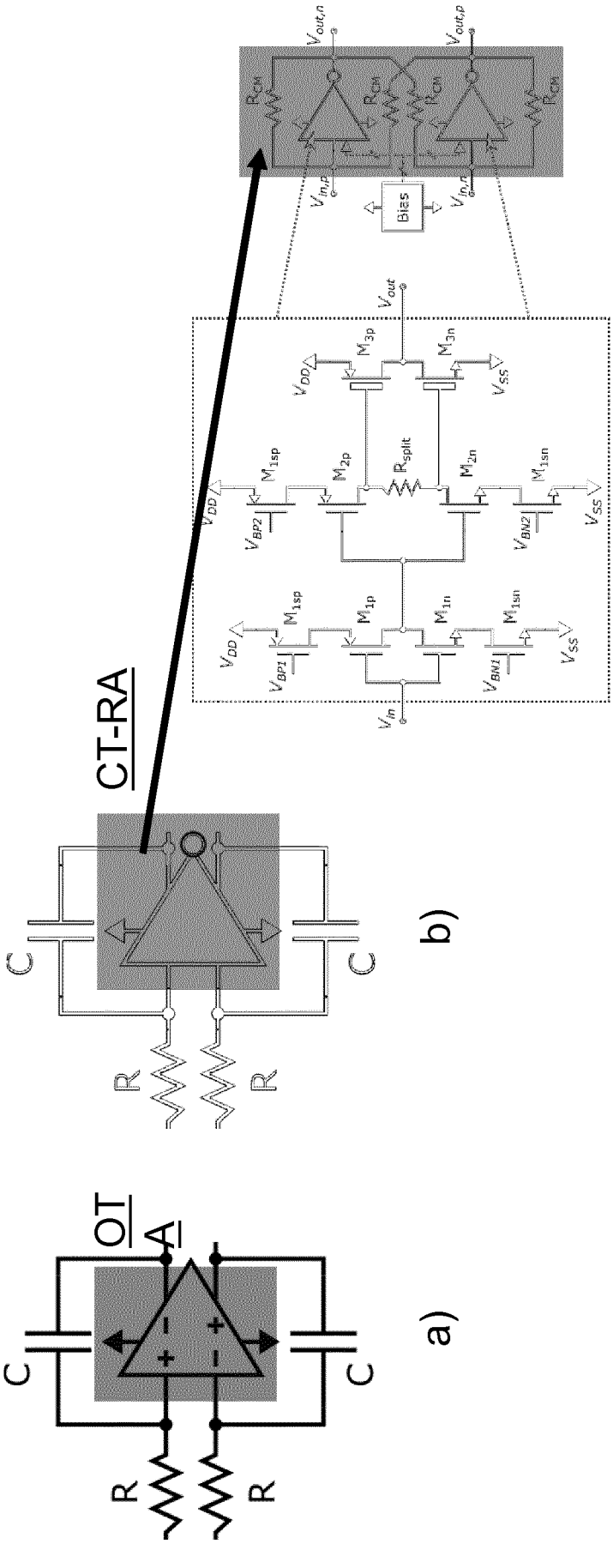


FIG. 14

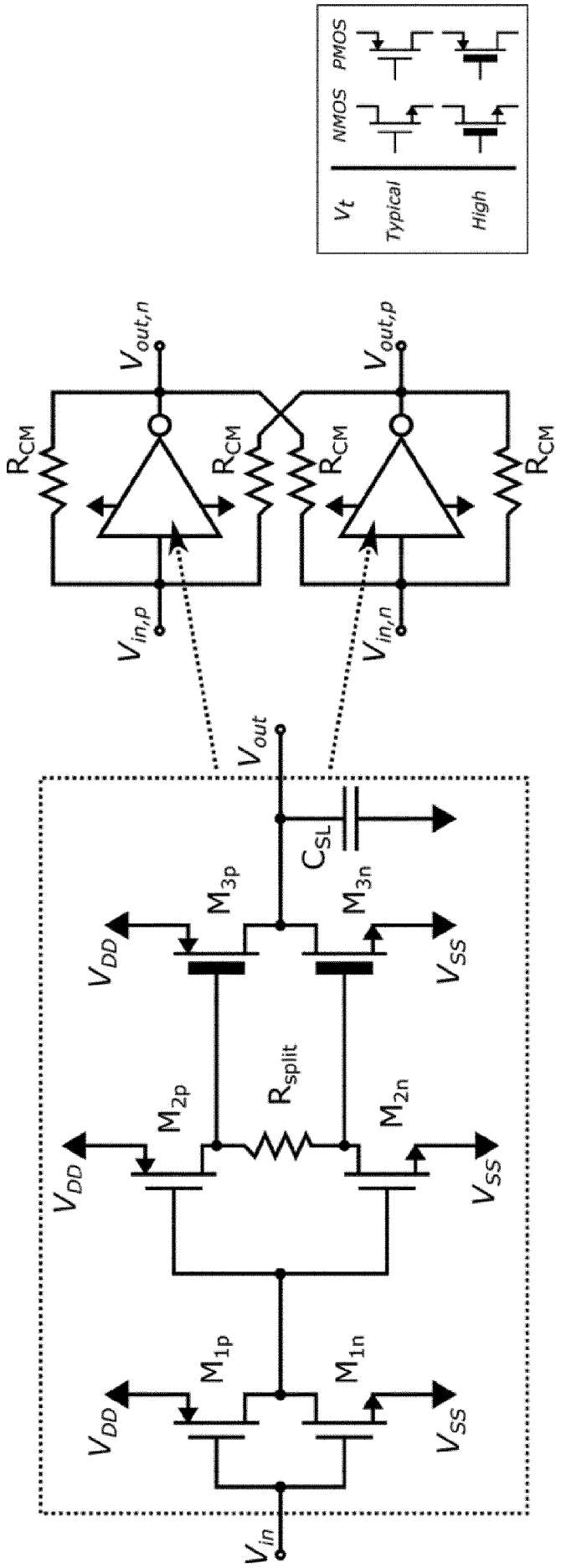

PMOS
NMOS
V_t
Typical
High
$V_{out,n}$
$V_{out,p}$
R_{CM}
R_{CM}
R_{CM}
R_{CM}
$V_{in,p}$
$V_{in,n}$
V_{out}
C_{SL}
M_{3p}
M_{3n}
V_{DD}
V_{SS}
M_{2p}
R_{split}
M_{2n}
V_{DD}
V_{SS}
M_{1p}
M_{1n}
V_{DD}
V_{SS}
V_{in}

FIG. 15

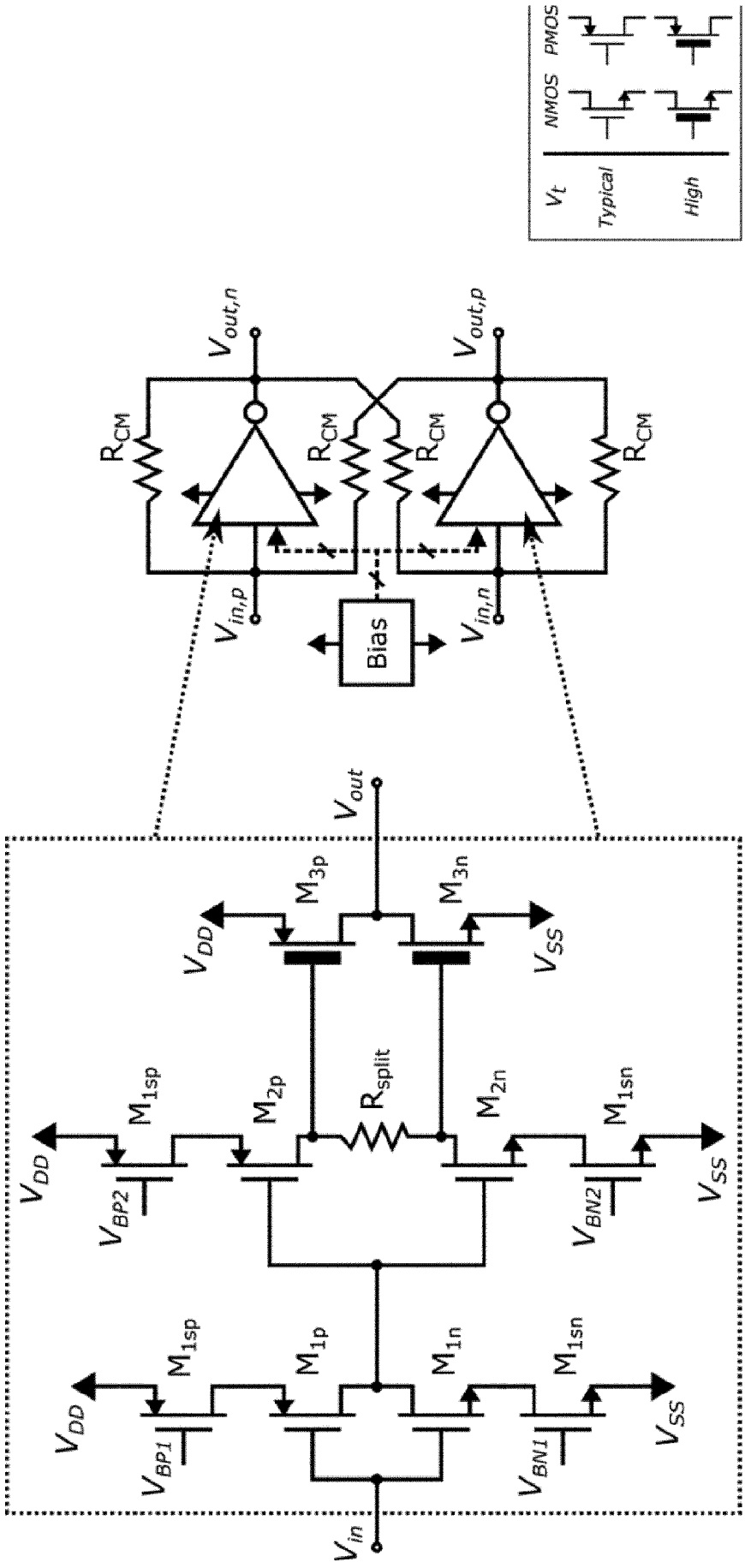

PMOS
NMOS
Vt
Typical
High
Vout,n
Vout,p
RCM
Vin,p
Vin,n
Bias
Vout
M3p
M3n
VDD
VSS
M1sp
M2p
Rsplit
M2n
M1sn
VBP2
VBN2
M1p
M1n
VBP1
VBN1
Vin

FIG. 16

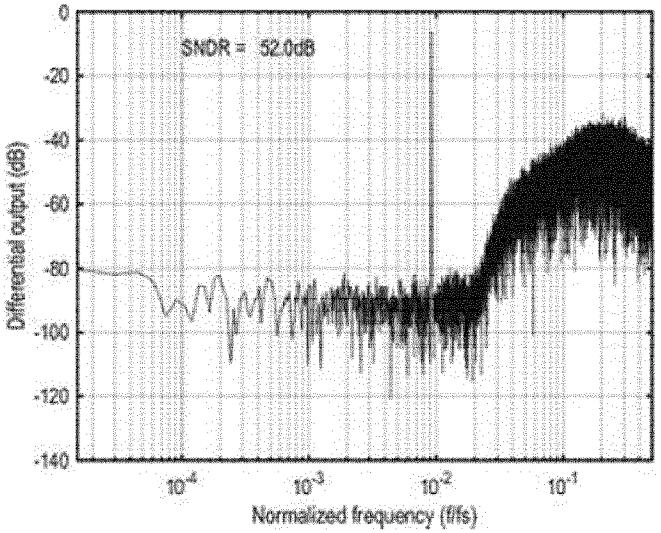


FIG. 17A

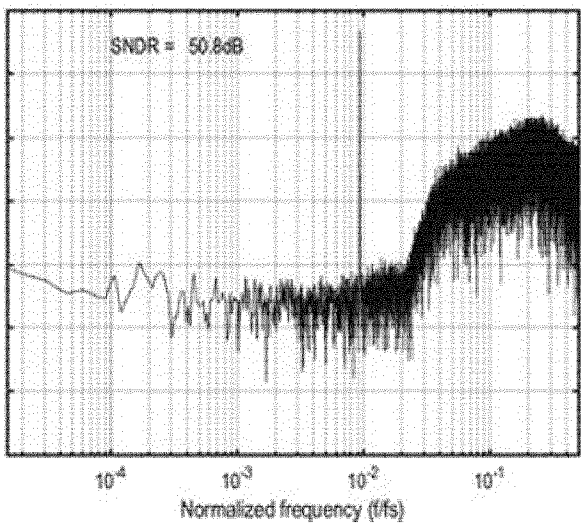


FIG. 17B

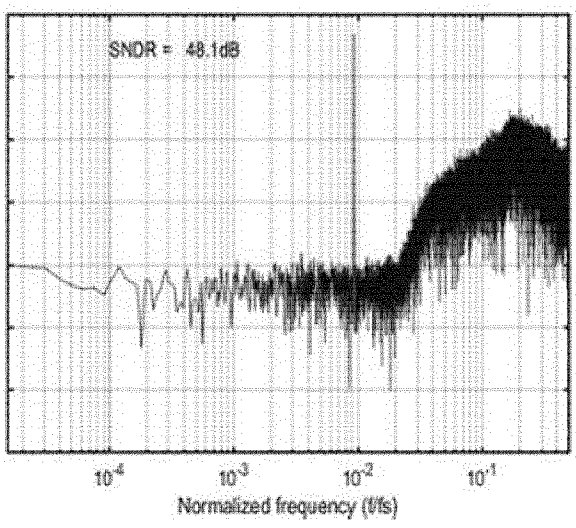


FIG. 17C

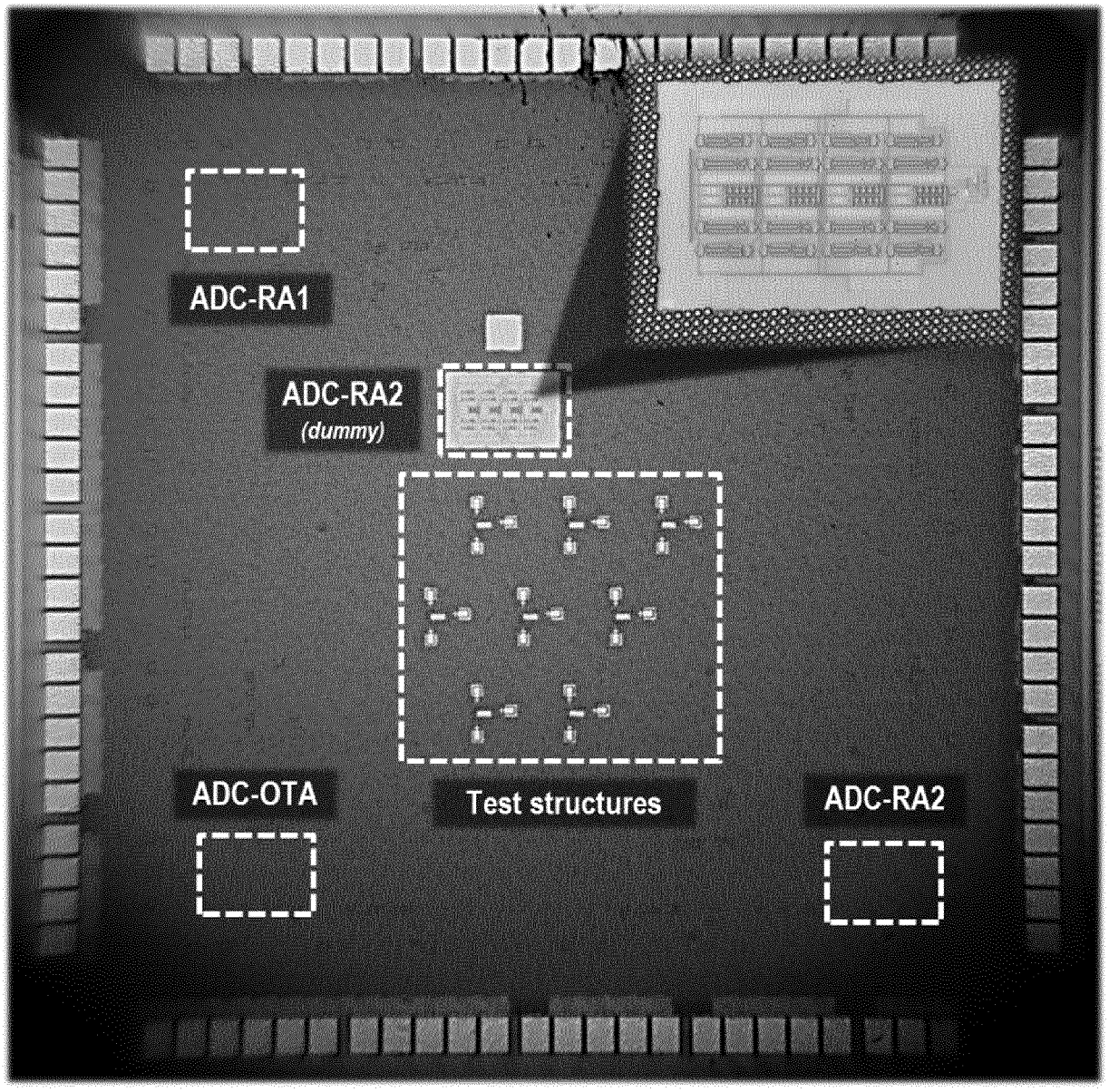


FIG. 18

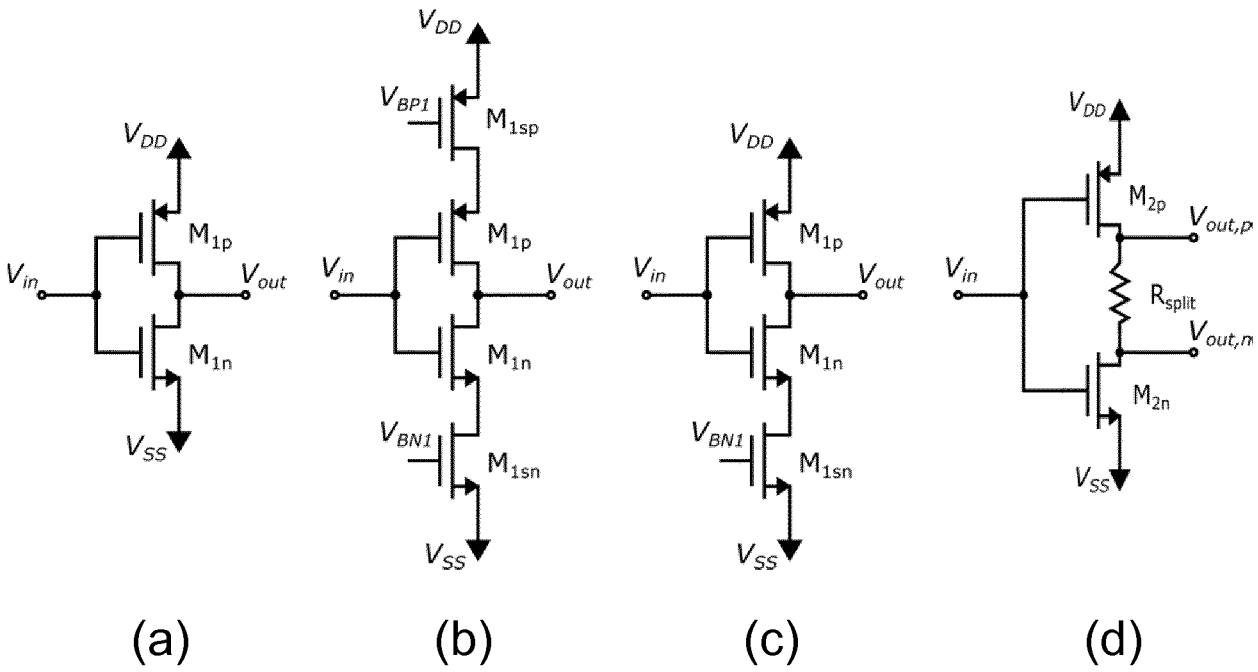

V_{DD}
M_{1p}
V_{in}
V_{out}
M_{1n}
V_{SS}
(a)
V_{DD}
V_{BP1}
M_{1sp}
M_{1p}
V_{in}
V_{out}
M_{1n}
V_{BN1}
M_{1sn}
V_{SS}
(b)
V_{DD}
M_{1p}
V_{in}
V_{out}
M_{1n}
V_{BN1}
M_{1sn}
V_{SS}
(c)
V_{DD}
M_{2p}
$V_{out,p}$
V_{in}
R_{split}
$V_{out,n}$
M_{2n}
V_{SS}
(d)

FIG. 19

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/075973

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/30 H03F3/187 H03F3/26 H03F3/45 H03F3/60
H03M3/00
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal , WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Benjamin Hershberg ET AL: "The Ring Amplifier: Scalable Amplification with Ring Oscillators" In: "High-Performance AD and DA Converters , IC Design in Scaled Technologies, and Time-Domain Signal Processing", 1 January 2015 (2015-01-01) , Springer International Publishing, Cham, XP055455307 , ISBN: 978-3-319-07938-7 pages 399-418, DOI: 10.1007/978-3-319-07938-7_18, figures 1,2,9 pages 1-5 pages 12-14 pages 17-22 --- -/-	1-15

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" documentwhich may throw doubts on priority claim(s) orwhich is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 November 2018	03/12/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Jespers , Michael

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	LIM YONG ET AL: "A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 50, no. 10, 1 October 2015 (2015-10-01), pages 2331-2341, XP011670378, ISSN: 0018-9200, DOI: 10.1109/JSSC.2015.2453332 [retrieved on 2015-09-28] figures 1-10 page 2331, right-hand column, line 38 - page page 2336, left-hand column, line 38	1-15
X	CA0 YUEFENG ET AL: "An improved ring amplifier with process- and supply voltage-insensitive dead-zone", 2017 IEEE 60TH INTERNATIONAL MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS (MWSCAS), IEEE, 6 August 2017 (2017-08-06), pages 811-814, XP033158147, DOI: 10.1109/MWSCAS.2017.8053047 [retrieved on 2017-09-27] figures 1-7 page 811, left-hand column, line 1 - page 814, right-hand column, line 16	1-15
X	SUGUR0 TAKUMA ET AL: "Low power DT delta-sigma modulator with ring amplifier SC-integrator", 2016 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (ISCAS), IEEE, 22 May 2016 (2016-05-22), pages 2006-2009, XP032941976, DOI: 10.1109/ISCAS.2016.7538970 [retrieved on 2016-08-09] page 2006, left-hand column, line 1 - page 2007, left-hand column, line 23 figure 4	1-15
A	ESSAWY A ET AL: "A low voltage inverter-based continuous-time sigma delta analog-to-digital converter in 65nm CMOS technology", 2014 IEEE FAIBLE TENSION FAIBLE CONSOMMATION, IEEE, 4 May 2014 (2014-05-04), pages 1-4, XP032605579, DOI: 10.1109/FTFC.2014.6828599 abstract figures 3,5,6 page 1, left-hand column, line 1 - page 3, left-hand column, line 30	1-15

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ISMAI L AYMAN ET AL: "A Process-Tol erant, Low-Vol tage, Inverter-Based OTA for Conti nuous-Time $\Si gma $ - $\Del t a $ ADC" , I EEE'TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, I EEE SERVICE CENTER, PISCATAWAY, NJ , USA, vol . 24, no. 9 , 1 September 2016 (2016-09-01) , pages 2911-2917 , XP011620537 , ISSN : 1063-8210, D0I : 10. 1109/TV LSI . 2016. 2525786 [retri eved on 2016-08-23] abstract page 10 page 2911 , l eft-hand col umn , l i ne 18 - page 2912 , l eft-hand col umn , l i ne 26	1-15
A	Franco Mal oberti : "CMOS Comparators Anal og Integrated Ci rcui t Desi gn" , , 5 November 2014 (2014-11-05) , XP055454426, Retri eved from the Internet: URL: http ://ims . uni pv . i t/Courses/downl oad/A I C/Presentati onN006.pdf [retri eved on 2018-02-26] page 14 - page 16	1-15